

In the claims:

1 1. (Cancelled) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core;
3 identifying an application;
4 designing an application specific circuit for the application; and
5 integrating the programmable logic core into the designed application specific
6 circuit.

1 2. (Cancelled) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core for the integrated circuit;
3 establishing a set of timing constraints associated with the programmable
4 logic core; and
5 controlling the design of application specific circuitry that interfaces with the
6 programmable logic core in the integrated circuit in accordance with the set of timing
7 constraints.

1 3. (Cancelled) A method of designing an integrated circuit, comprising:
2 identifying a programmable logic core for the integrated circuit;
3 establishing a sign-off design associated with the programmable logic core;
4 and
5 controlling the design of application specific circuitry that interfaces with the
6 programmable logic core in the integrated circuit in accordance with the sign-off design.

1 4. (Cancelled) An integrated circuit, comprising;
2 a programmable logic core; and
3 application specific circuitry, the application specific circuitry being designed
4 in accordance with a sign-off design.

1 5. (Cancelled) An integrated circuit according to claim 4, wherein the programmable
2 logic core includes:
3 a programmable multi-scale array;
4 an application circuit interface for providing a signal interface between the
5 programmable multi-scale array and the application specific circuitry; and
6 a programmable logic core adapter that configures the programmable multi-
7 scale array.

1 6. (Cancelled) The integrated circuit of claim 5, wherein the programmable multi-
2 scale array comprises an array of configurable arithmetic logic units supporting at least:
3 register transfer level functions; and
4 random logic structures.

1 7. (Cancelled) The integrated circuit according to claim 4, wherein the programmable
2 logic core comprises a programmable multi-scale array supporting functions of different
3 scales.

1 8. (Cancelled) The integrated circuit according to claim 4, wherein the programmable
2 logic core includes at a programmable logic core control for loading configuration data into
3 the programmable logic core.

1 9. (Cancelled) The integrated circuit according to claim 4, wherein the programmable
2 logic core comprises:
3 an array of configurable logic structures having internal storage registers; and
4 a scratchpad memory to supplement the storage registers.

1 10. (Cancelled) The integrated circuit according to claim 4, wherein the
2 programmable logic core includes at a configuration test interface for data and control flow
3 between the application specific circuit and the programmable logic core.

1 11. (Cancelled) The integrated circuit according to claim 4 further comprising a
2 microprocessor core communicatively connected to the programmable logic core.

1 12. (Cancelled) The integrated circuit according to claim 4, wherein the
2 programmable logic core comprises blocks supporting:
3 configuration data control logic;
4 scan path logic; and
5 application circuit interface logic.

1 13. (Cancelled) The integrated circuit according to claim 4, wherein the
2 programmable logic core comprises arithmetic logic units including:
3 function cells; and
4 an arithmetic logic unit controller.

1 14. (Cancelled) The integrated circuit according to claim 4, wherein the
2 programmable logic comprises:
3 an internet protocol core; and
4 arithmetic logic units communicatively connected to the internet protocol core.

1 15. (Previously presented) An integrated circuit, comprising:
2 a programmable logic core that supports:
3 an idle state that is entered after an assertion of a signal that power is good;
4 a built in self test state for testing the programmable logic core, the built in
5 self test state is entered from the idle state upon receipt of a test
6 command;
7 a configuration state for implementing a configuration process, the
8 configuration state supports entry from the idle state and from the built
9 in self test state after receipt of a configuration clock signal; and
10 an operate state that controls operations of arithmetic logic units, and is
11 entered after completion of the configuration process; and
12 application specific circuitry, the application specific circuitry being designed in
13 accordance with a sign-off design.

1 16. (Cancelled) An integrated circuit, comprising;
2 means for performing functions associated with a programmable logic core; and
3 means for performing functions associated with application specific circuitry that is
4 designed in accordance with a sign-off design.

- 1 17. (Previously Presented) An integrated circuit, comprising:
- 2 (I) application specific circuitry, the application specific circuitry being designed in
- 3 accordance with a sign-off design; and
- 4 (II) a first programmable logic core including at least
- 5 (A) a programmable multi-scale array having an array of configurable
- 6 arithmetic logic units supporting register transfer level functions, random
- 7 logic structures, and state machine structures,
- 8 (B) an application circuit interface for providing a signal interface between the
- 9 programmable multi-scale array and the application specific circuitry, the
- 10 application circuit interface having test registers for testing the
- 11 programmable logic core,
- 12 (C) scratchpad memories for supplementing storage of the programmable
- 13 multi-scale array,
- 14 (D) a configuration test interface for data and control flow between the
- 15 application specific circuit and the programmable multi-scale array,
- 16 (E) a programmable logic control for loading configuration data into the
- 17 multi-scale array, and
- 18 (F) a programmable logic core adapter that configures the programmable
- 19 multi-scale array through the configuration test interface.

1 19. (Previously presented) The integrated circuit according to claim 15, wherein the
2 first programmable logic core comprises:
3 a programmable multi-scale array comprising a plurality of configurable
4 arithmetic logic units; and
5 a programmable logic core adapter that configures the programmable multi-
6 scale array.

1 20. (Previously presented) The integrated circuit according to claim 15, wherein the
2 programmable logic core adapter is configured to receive configuration data and load the
3 configuration data into configuration memory of the programmable logic core adapter.

1 21. (Previously presented) The integrated circuit according to claim 15, wherein the
2 first programmable logic core comprises an application circuit interface that interfaces
3 between the programmable multi-scale array and the application specific circuitry.

1 22. (Previously presented) The integrated circuit according to claim 15, wherein the
2 programmable multi-scale array performs register transfer level functions.

1 23. (Previously presented) The integrated circuit according to claim 15, further
2 comprising a plurality of other programmable logic cores.

1 24. (Previously presented) The integrated circuit according to claim 15, wherein the
2 first programmable logic core includes a programmable logic core control for controlling the
3 programmable logic core.

1 25. (Previously presented) The integrated circuit according to claim 24, wherein the
2 programmable logic core control provides a control mechanism for testing the first
3 programmable logic core.

1 26. (Previously presented) The integrated circuit according to claim 15, further
2 comprising scratchpad memory.

1 27. (Previously presented) The integrated circuit according to claim 17, further
2 comprising a configuration data source that stores the configuration data.

1 28. (Previously presented) The integrated circuit according to claim 17, further
2 comprising a plurality of other programmable logic cores.

1 29. (Previously presented) The integrated circuit according to claim 17, wherein the
2 programmable logic core control provides a control mechanism for testing the first
3 programmable logic core.